Fig. 1

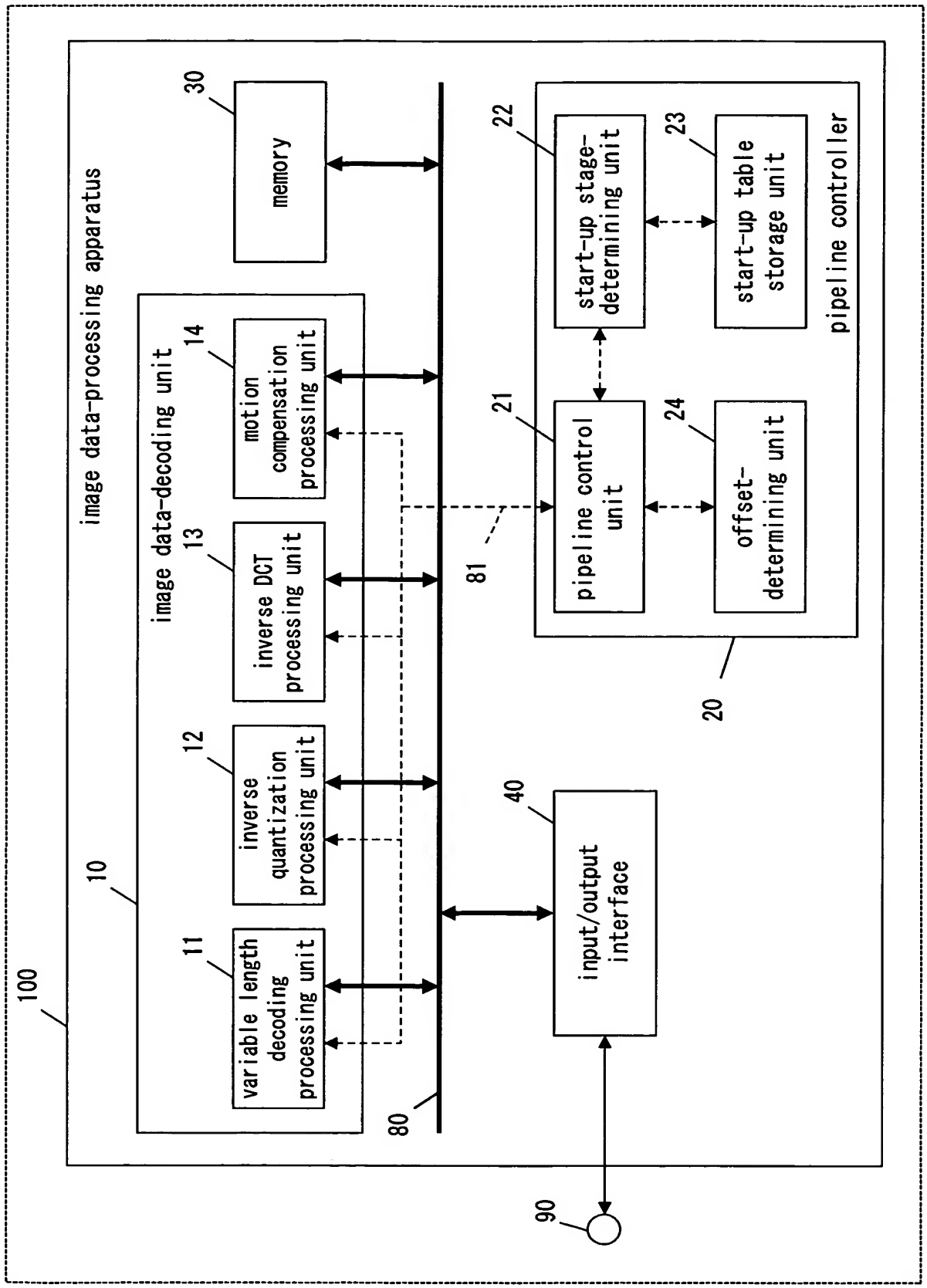

100
image data-processing apparatus
10
image data-decoding unit
11
variable length decoding processing unit
12
inverse quantization processing unit
13
inverse DCT processing unit
14
motion compensation processing unit
30
memory
80
40
input/output interface
90
20
pipeline controller
21
pipeline control unit
22
start-up stage-determining unit
23
start-up table storage unit
24
offset-determining unit
81

Fig. 2(a)

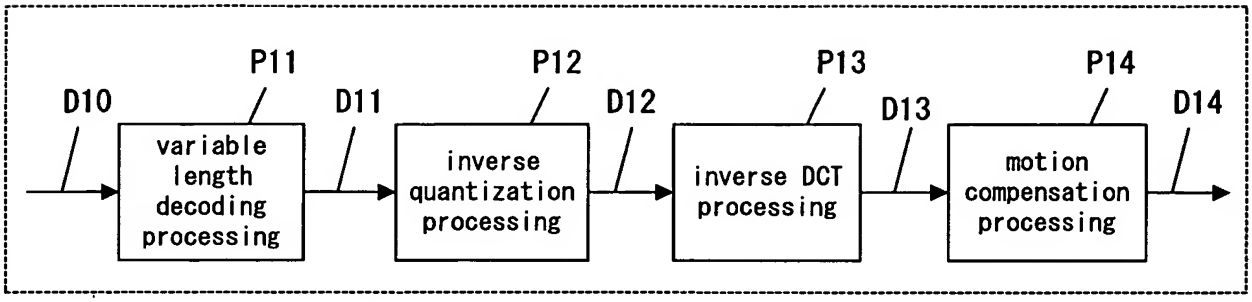

D10
P11
variable length decoding processing
D11
P12
inverse quantization processing
D12
P13
inverse DCT processing
D13
P14
motion compensation processing
D14

Fig. 2(b)

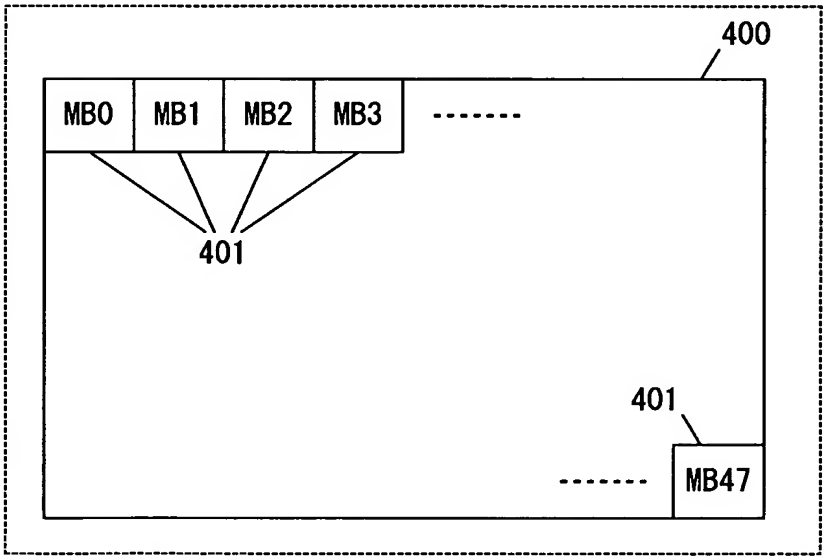

400
MB0
MB1
MB2
MB3
401
401
MB47

Fig. 3

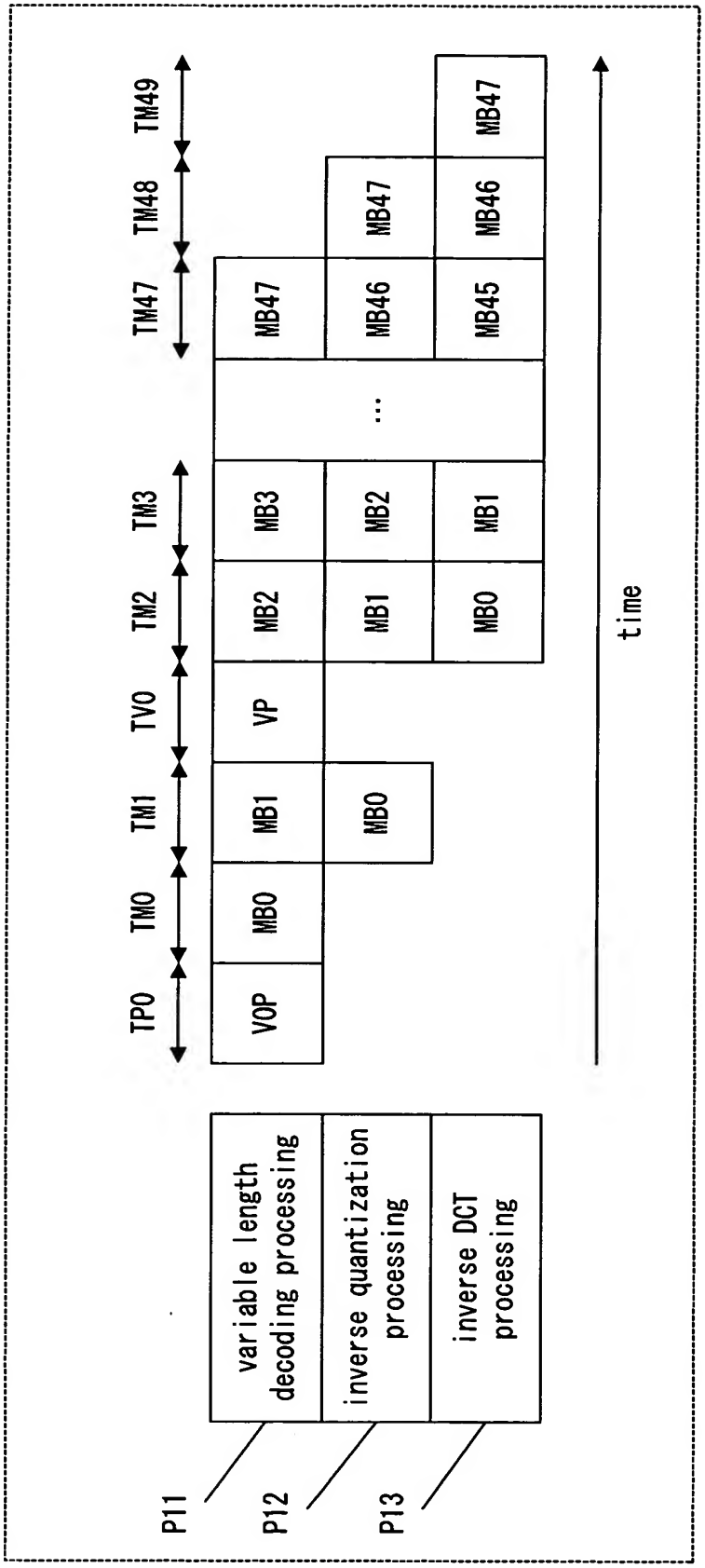

TP0
TM0
TM1
TV0
TM2
TM3
TM47
TM48
TM49
VOP
MB0
MB1
VP
MB2
MB3
MB47
MB0
MB1
MB2
MB46
MB47
MB0
MB1
MB45
MB46
MB47
...
time
P11
P12
P13
variable length decoding processing
inverse quantization processing
inverse DCT processing

Fig. 4

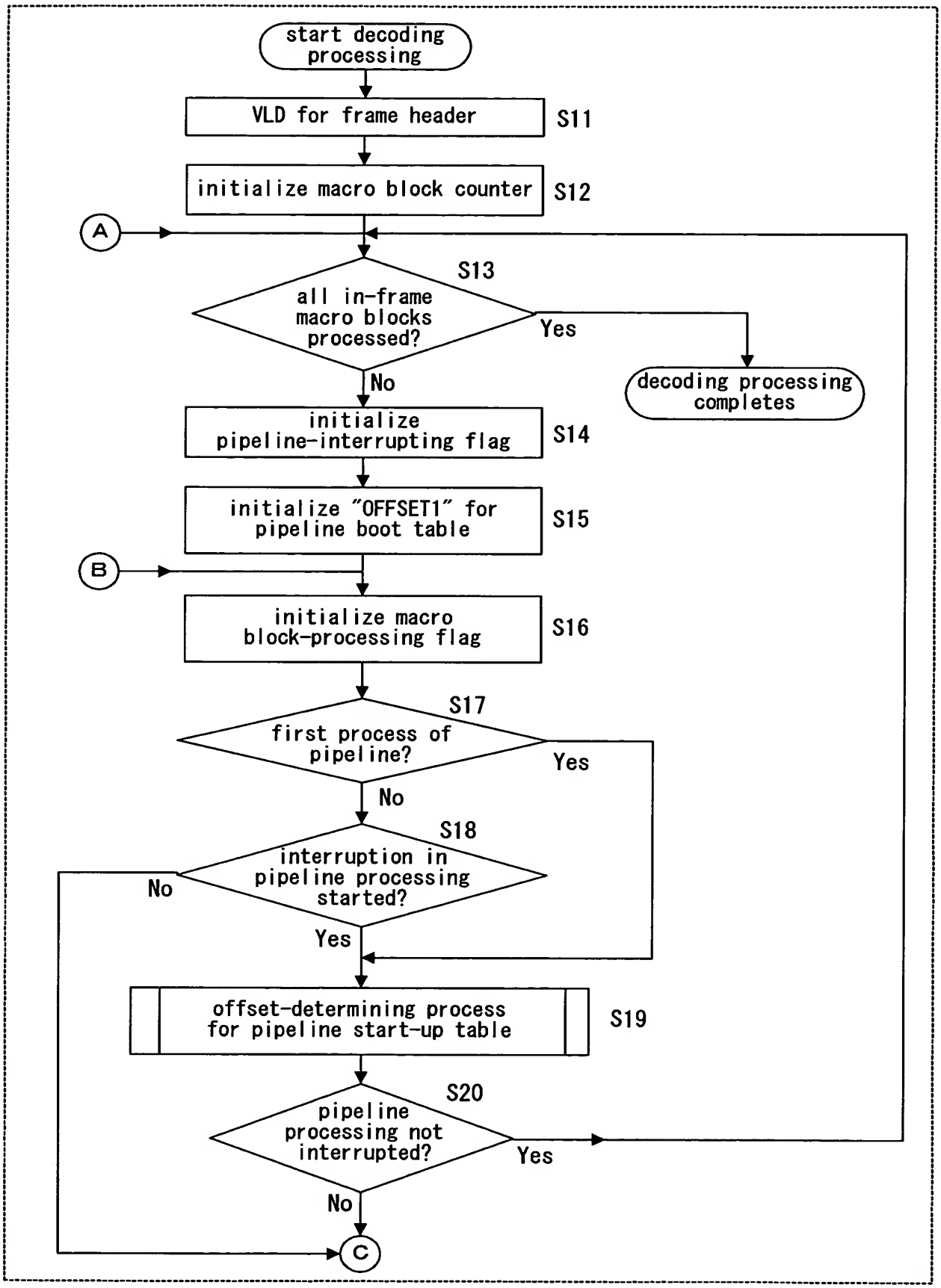

start decoding processing
VLD for frame header
S11
initialize macro block counter
S12
A
S13
all in-frame macro blocks processed?
Yes
decoding processing completes
No
initialize pipeline-interrupting flag
S14
initialize "OFFSET1" for pipeline boot table
S15
B
initialize macro block-processing flag
S16
S17
first process of pipeline?
Yes
No
S18
interruption in pipeline processing started?
No
Yes
offset-determining process for pipeline start-up table
S19
S20
pipeline processing not interrupted?
Yes
No
C

Fig. 5

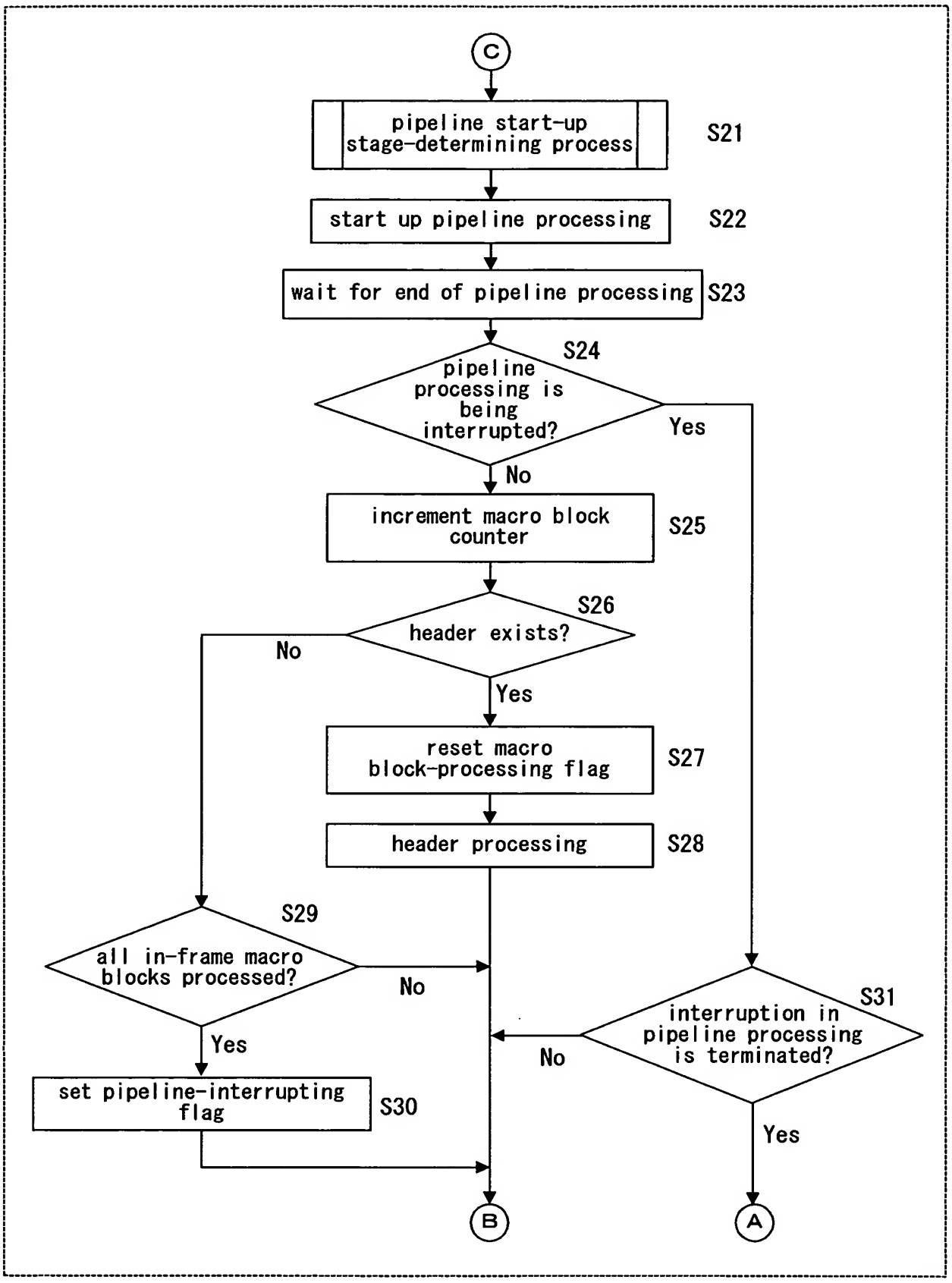

C
pipeline start-up stage-determining process
S21
start up pipeline processing
S22
wait for end of pipeline processing
S23
S24
pipeline processing is being interrupted?
Yes
No
increment macro block counter
S25
S26
header exists?
No
Yes
reset macro block-processing flag
S27
header processing
S28
S29
all in-frame macro blocks processed?
No
Yes
set pipeline-interrupting flag
S30
S31
interruption in pipeline processing is terminated?
No
Yes
B
A

Fig. 6

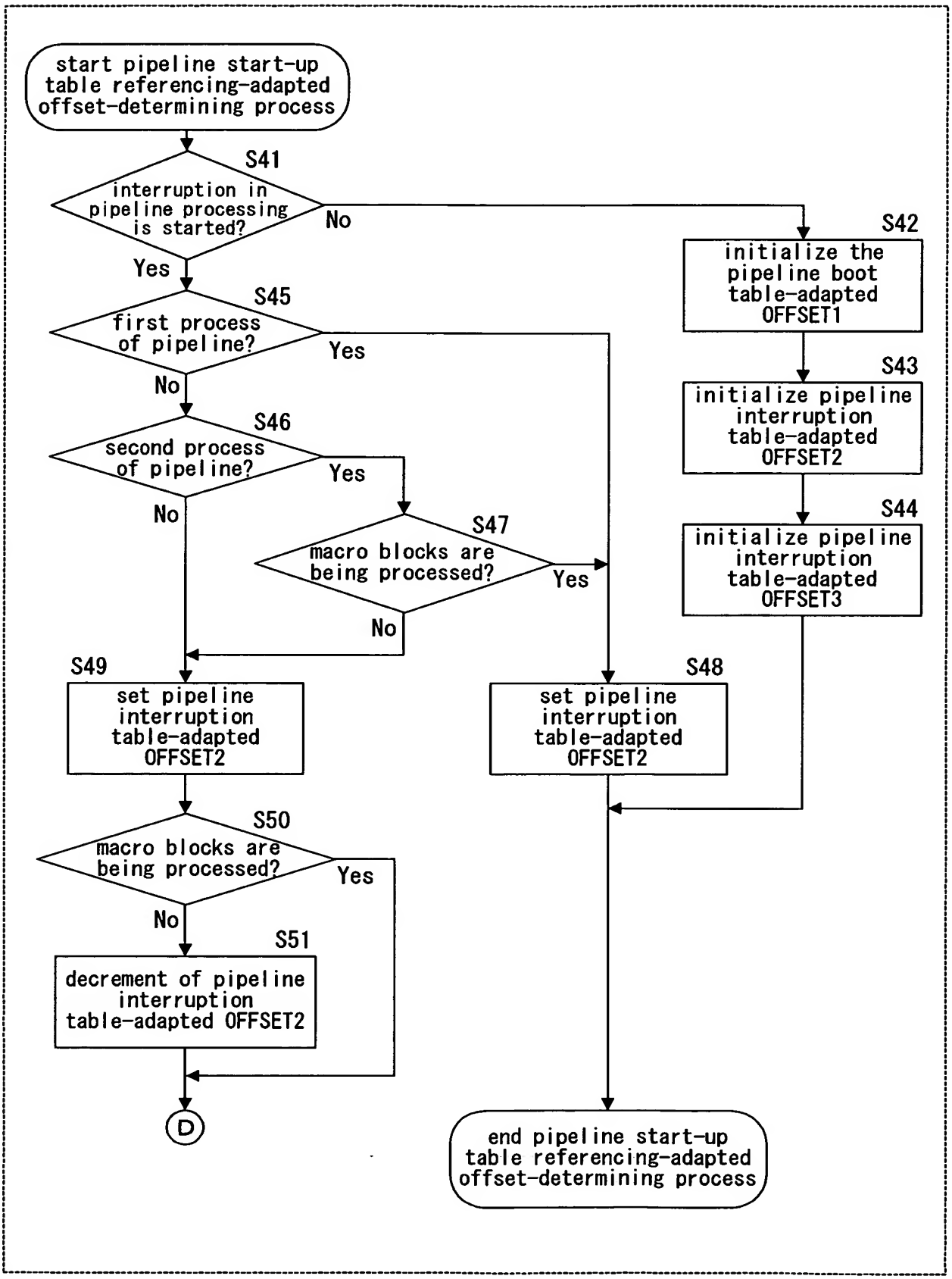

start pipeline start-up table referencing-adapted offset-determining process
S41
interruption in pipeline processing is started?
No
Yes
S42
initialize the pipeline boot table-adapted OFFSET1
S43
initialize pipeline interruption table-adapted OFFSET2
S44
initialize pipeline interruption table-adapted OFFSET3
S45
first process of pipeline?
Yes
No
S46
second process of pipeline?
Yes
No
S47
macro blocks are being processed?
Yes
No
S48
set pipeline interruption table-adapted OFFSET2
S49
set pipeline interruption table-adapted OFFSET2
S50
macro blocks are being processed?
Yes
No
S51
decrement of pipeline interruption table-adapted OFFSET2
D
end pipeline start-up table referencing-adapted offset-determining process

Fig. 7

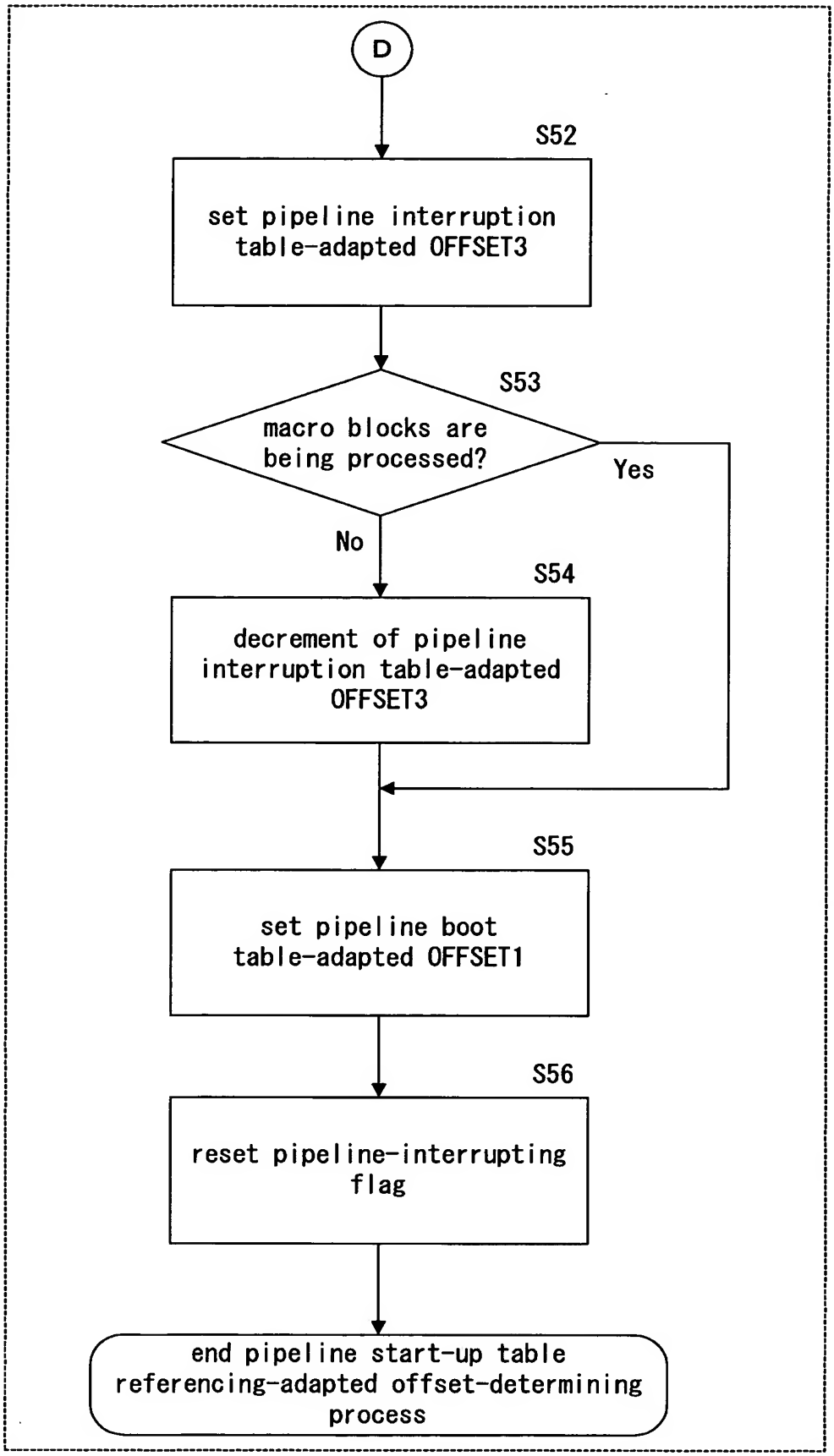

D
S52
set pipeline interruption table-adapted OFFSET3
S53
macro blocks are being processed?
Yes
No
S54
decrement of pipeline interruption table-adapted OFFSET3
S55
set pipeline boot table-adapted OFFSET1
S56
reset pipeline-interrupting flag
end pipeline start-up table referencing-adapted offset-determining process

Fig. 8

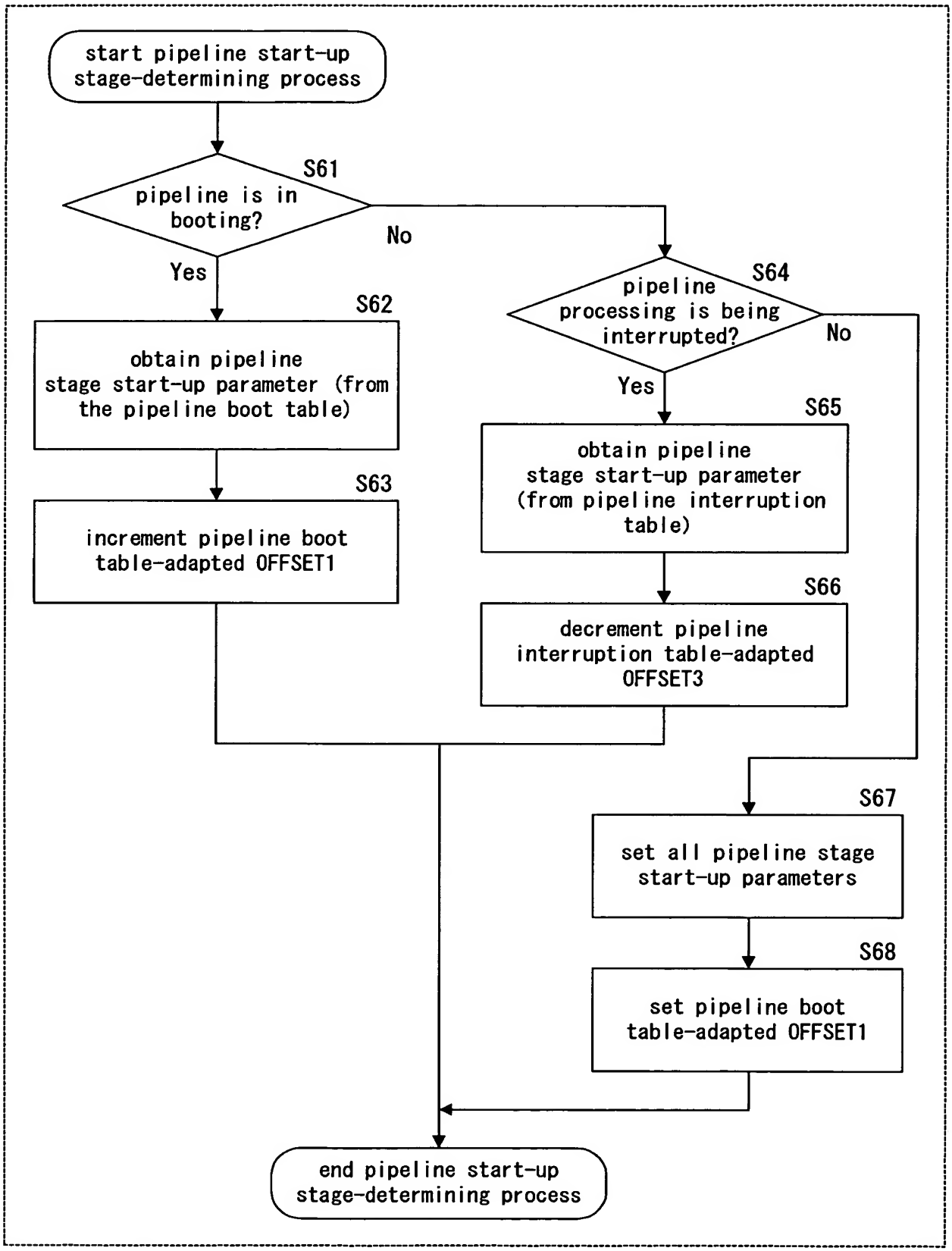

start pipeline start-up stage-determining process
S61
pipeline is in booting?
No
Yes
S62
obtain pipeline stage start-up parameter (from the pipeline boot table)
S63
increment pipeline boot table-adapted OFFSET1
S64
pipeline processing is being interrupted?
No
Yes
S65
obtain pipeline stage start-up parameter (from pipeline interruption table)
S66
decrement pipeline interruption table-adapted OFFSET3
S67
set all pipeline stage start-up parameters
S68
set pipeline boot table-adapted OFFSET1
end pipeline start-up stage-determining process

Fig. 9 (a)

420

```
pipeline boot table
TABLE1[2] = {
_S1,
_S1|_S2
}
```

Fig. 9 (b)

421

```
pipeline interruption table
TABLE2[2][2] = {
{_S3,_S2},
{_S3, _S3|_S2}
}
```

Fig. 10

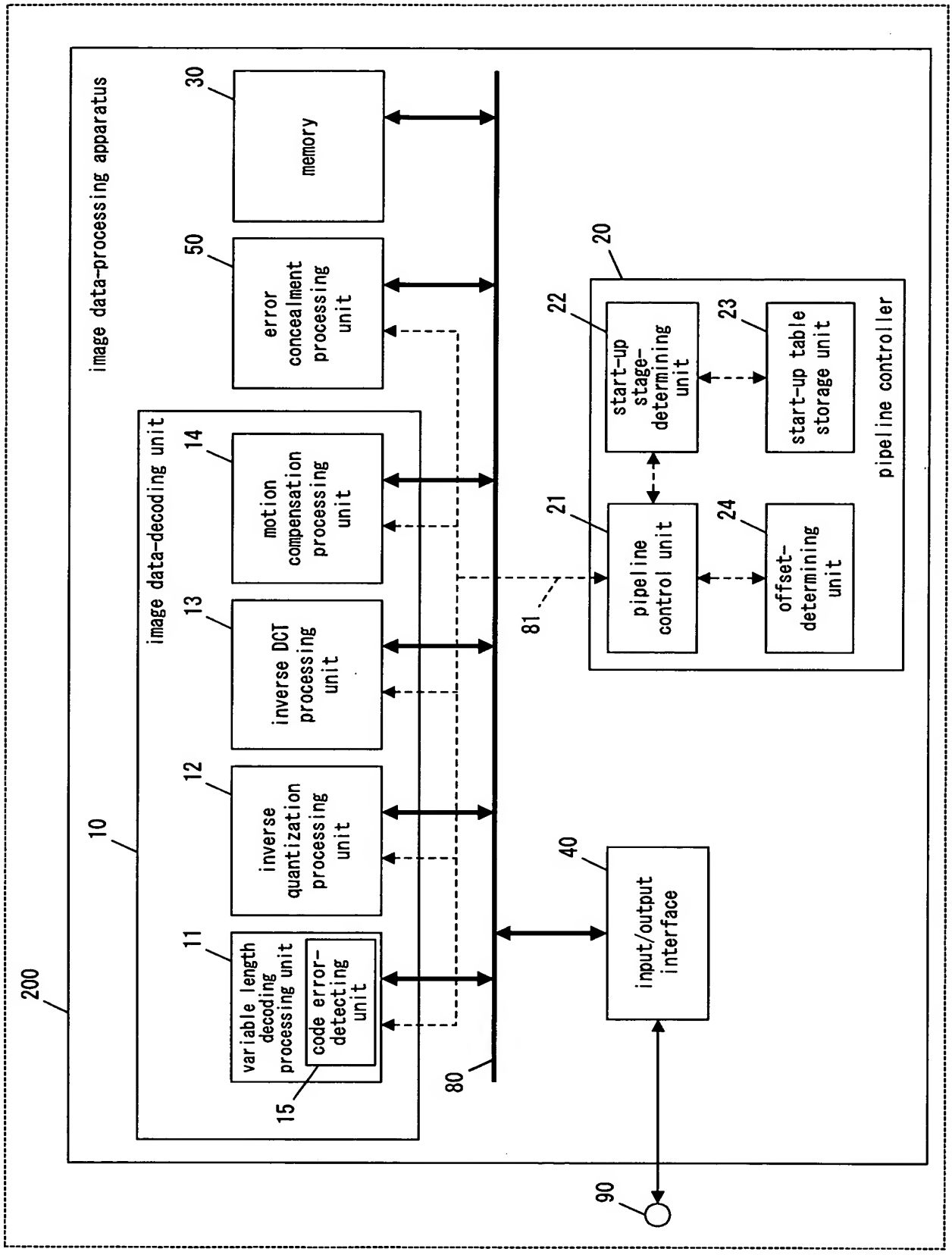

200
image data-processing apparatus
10
image data-decoding unit
11
variable length decoding processing unit
code error-detecting unit
15
12
inverse quantization processing unit
13
inverse DCT processing unit
14
motion compensation processing unit
30
memory
50
error concealment processing unit
80
40
input/output interface
90
20
pipeline controller
21
pipeline control unit
22
start-up stage-determining unit
23
start-up table storage unit
24
offset-determining unit
81

Fig. 11

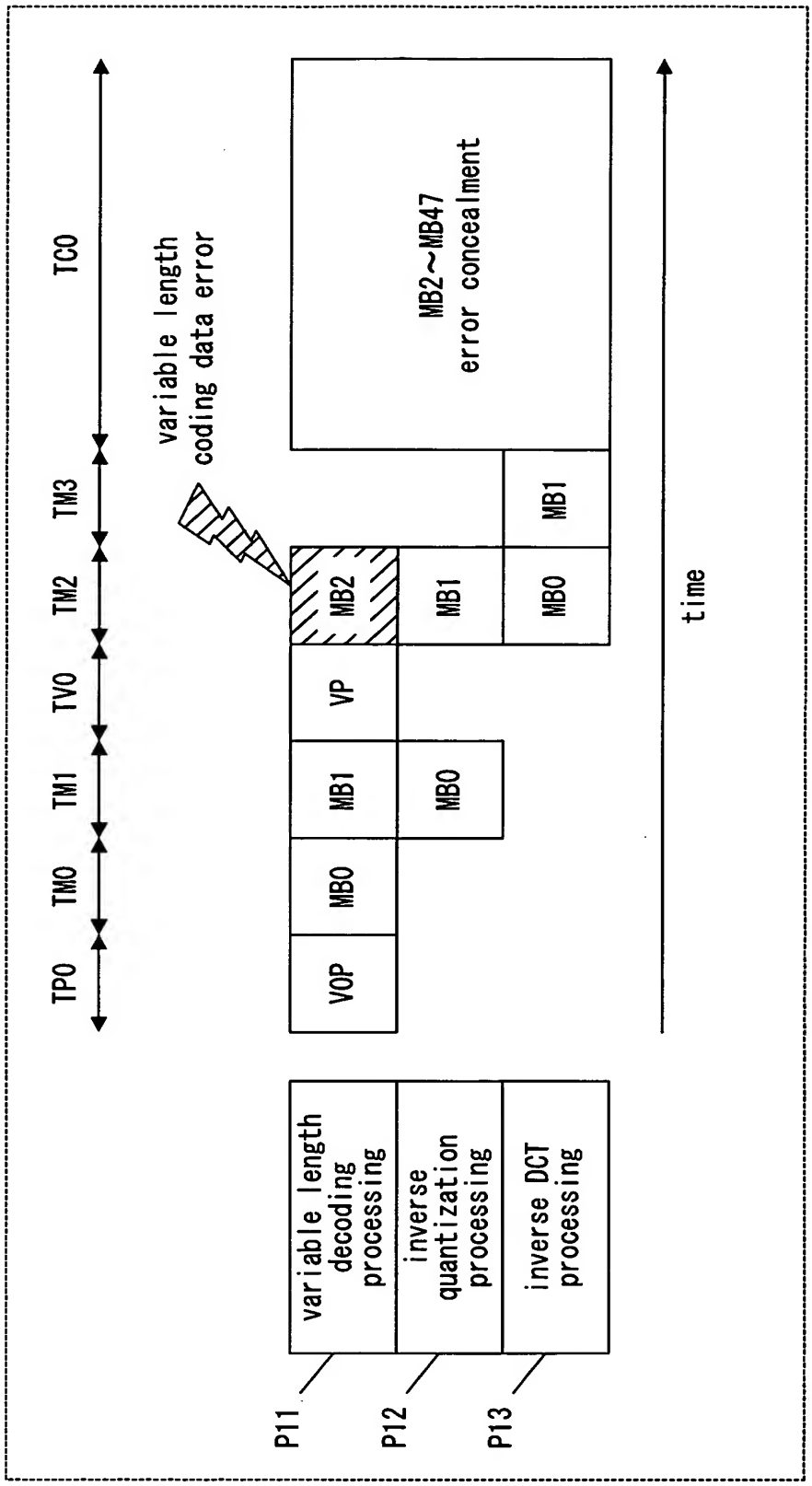

TP0
TM0
TM1
TV0
TM2
TM3
TC0
variable length coding data error
VOP
MB0
MB1
VP
MB2
MB0
MB1
MB0
MB1
MB2~MB47 error concealment
time
P11
P12
P13
variable length decoding processing
inverse quantization processing
inverse DCT processing

Fig. 12

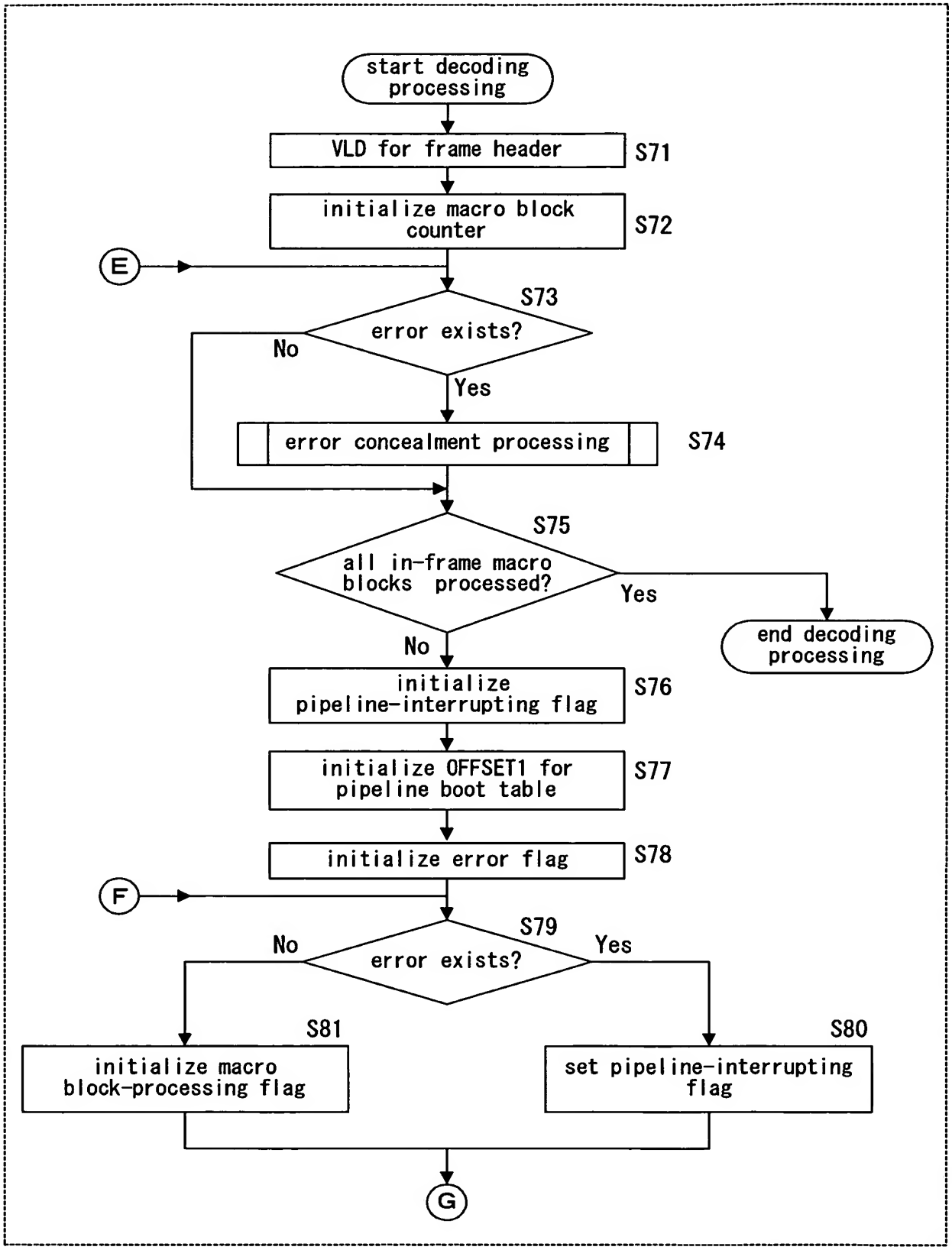

start decoding processing
VLD for frame header
S71
initialize macro block counter
S72
E
S73
error exists?
No
Yes
error concealment processing
S74
S75
all in-frame macro blocks processed?
Yes
end decoding processing
No
initialize pipeline-interrupting flag
S76
initialize OFFSET1 for pipeline boot table
S77
initialize error flag
S78
F
S79
No
error exists?
Yes
S81
initialize macro block-processing flag
S80
set pipeline-interrupting flag
G

Fig. 13

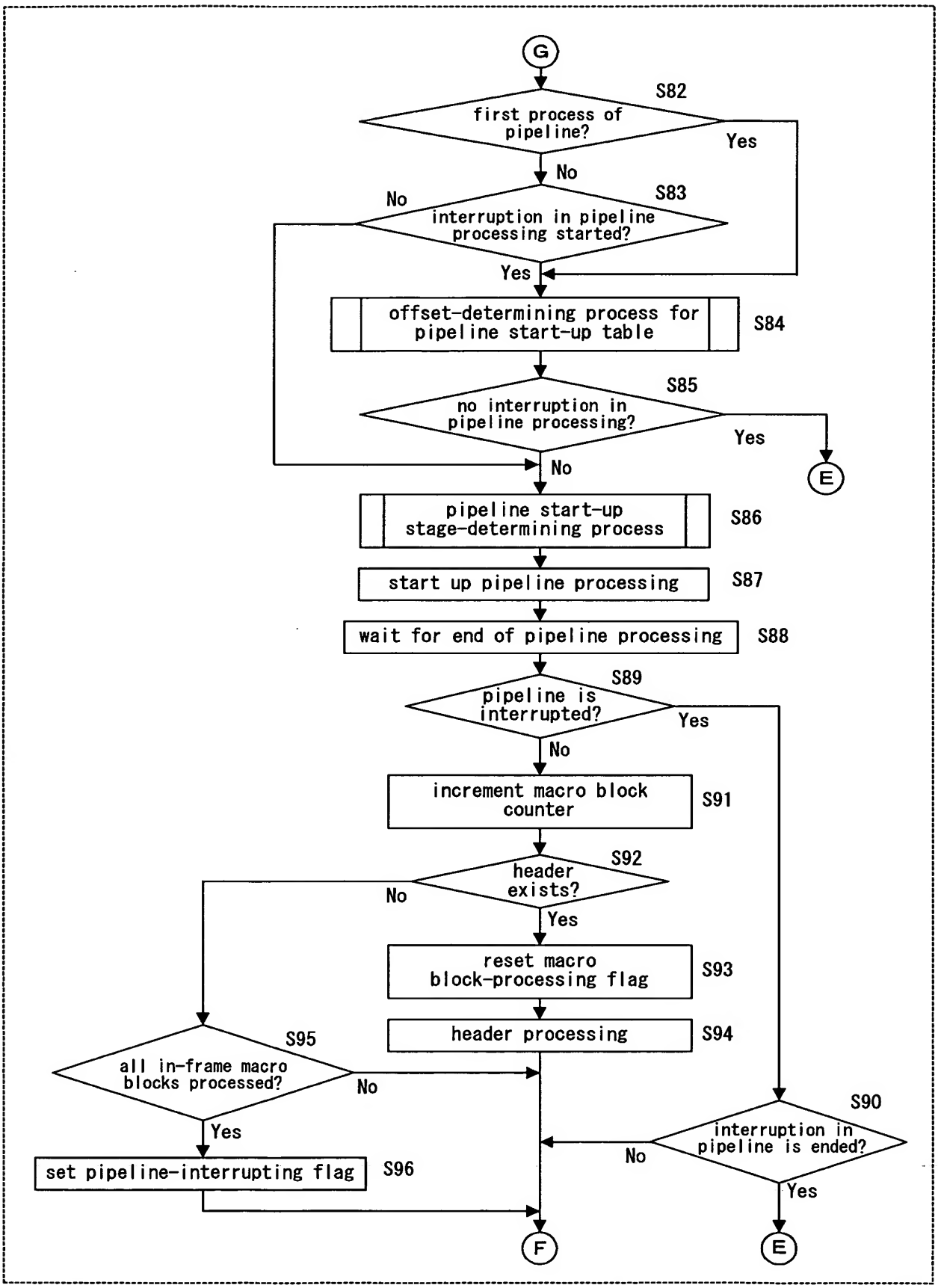

G
S82
first process of pipeline?
Yes
No
No
S83
interruption in pipeline processing started?
Yes
offset-determining process for pipeline start-up table
S84
S85
no interruption in pipeline processing?
Yes
E
No
pipeline start-up stage-determining process
S86
start up pipeline processing
S87
wait for end of pipeline processing
S88
S89
pipeline is interrupted?
Yes
No
increment macro block counter
S91
S92
header exists?
No
Yes
reset macro block-processing flag
S93
header processing
S94
S95
all in-frame macro blocks processed?
No
Yes
set pipeline-interrupting flag
S96
S90
interruption in pipeline is ended?
No
Yes
F
E

Fig. 14

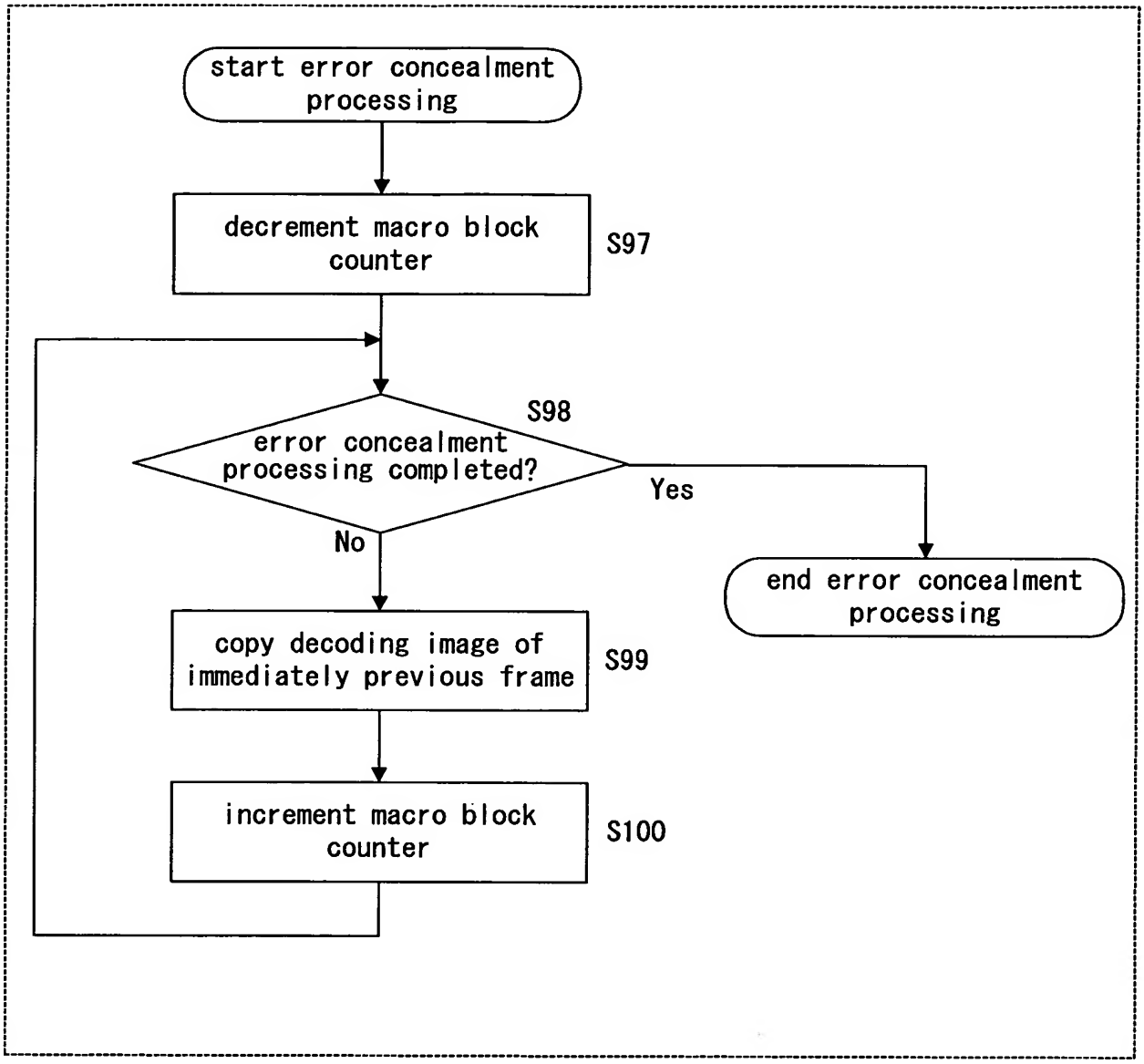

start error concealment processing
decrement macro block counter
S97
S98
error concealment processing completed?
Yes
No
end error concealment processing
copy decoding image of immediately previous frame
S99
increment macro block counter
S100

Fig. 15

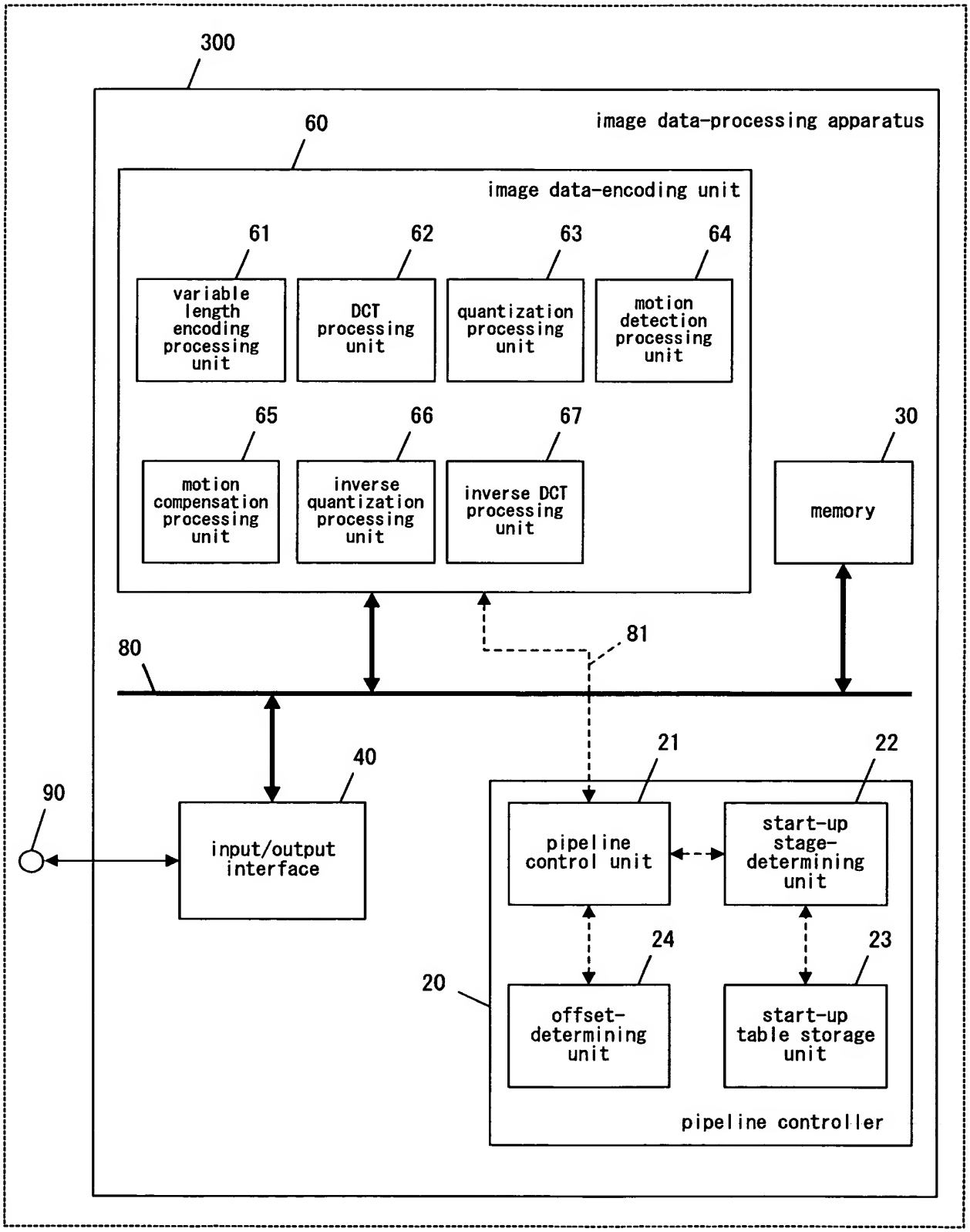

300
image data-processing apparatus
60
image data-encoding unit
61
variable length encoding processing unit
62
DCT processing unit
63
quantization processing unit
64
motion detection processing unit
65
motion compensation processing unit
66
inverse quantization processing unit
67
inverse DCT processing unit
30
memory
80
81
40
90
input/output interface
21
pipeline control unit
22
start-up stage-determining unit
24
23
20
offset-determining unit
start-up table storage unit
pipeline controller

Fig. 16

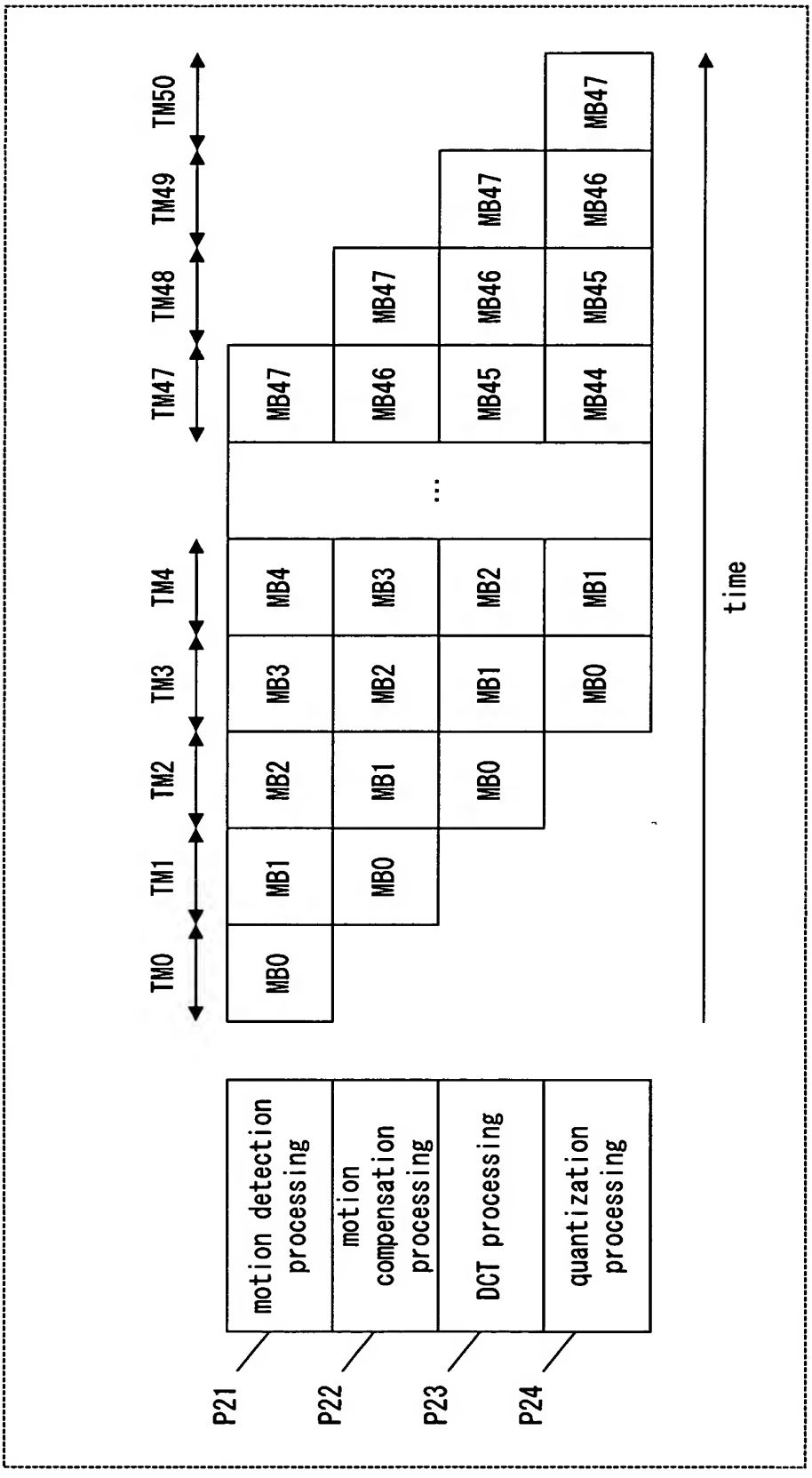
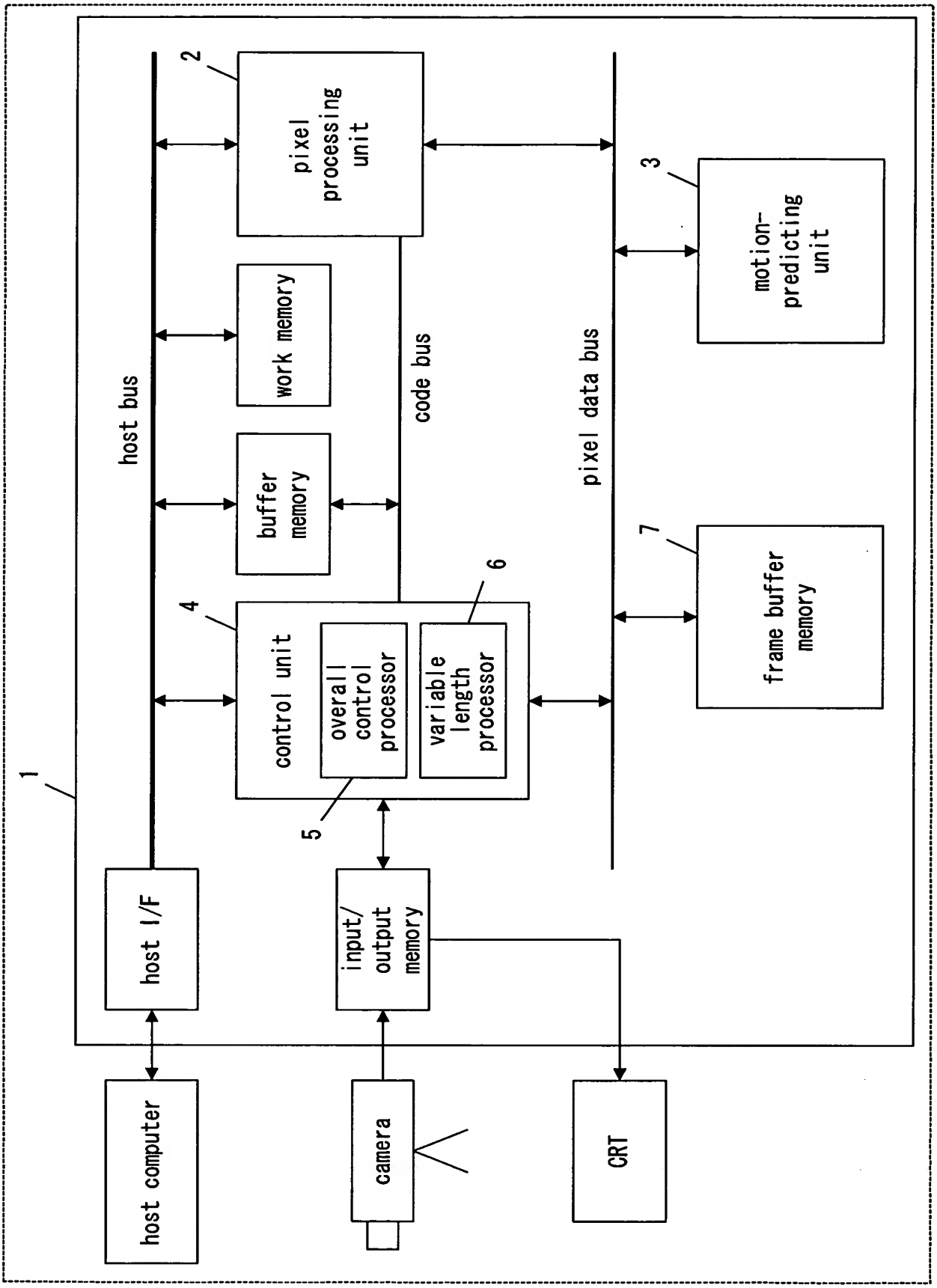

TM0
TM1
TM2
TM3
TM4
TM47
TM48
TM49
TM50
MB0
MB1
MB2
MB3
MB4
MB47
MB46
MB45
MB44
MB0
MB1
MB2
MB3
MB47
MB46
MB45
MB0
MB1
MB2
MB47
MB46
MB0
MB47
...
time
motion detection processing
motion compensation processing
DCT processing
quantization processing
P21
P22
P23
P24

Fig. 17


1
2
pixel processing unit
3
motion-predicting unit
work memory
buffer memory
host bus
code bus
pixel data bus
4
control unit
overall control processor
variable length processor
5
6
7
frame buffer memory
host I/F
input/output memory
host computer
camera
CRT